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KLARQUIST SPARKMAN, LLP
121 SW SALMON STREET
SUITE 1600
PORTLAND, OR 97204

EXAMINER	
STEVENS, THOMAS H	

ART UNIT	PAPER NUMBER
2121	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

MN

Office Action Summary	Application No.	Applicant(s)	
	09/883,836	BAILEY ET AL.	
	Examiner	Art Unit	
	Thomas H. Stevens	2121	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22 and 24-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5,7,12-21,24,30-33,35 and 36* is/are rejected.

7)☒ Claim(s) *4, 6,8-11,22, 25-29,34* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-22, 24-36 were examined.

Section I: RCE

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicants' submission filed on 05/08/2007 has been entered.

Section II: Non-Final Rejection

Claim Objections

3. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: claims 1 and 35 "first hardware component" and a "second hardware component"; claims 1,2,3,30-36 "first simulation model"' and a "second simulation model".

4. Claims 4, 6,8-11, 22, 25-29,34 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1 and 9 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. Claim 9 recites the limitation " the plurality of simulation domains " in line 1. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

9. Claims 1-3,5,7,12-21,24,30-33,35,36 are rejected under 35 U.S.C. 102(e) as being anticipated by Markov (US Patent 6,305,006; hereafter Markov). Markov teaches a method for electronic design.

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Claim 1. A method comprising: simulating a first hardware component (specification fails to define what a first hardware component, but the prior art teaches examples of hardware component, column 3, lines 38-42) in a circuit design (known software circuit simulation, e.g., HDL, VHDL, column 5, lines 15-24) with a first simulation model (the specification fails to define what a first simulation model is, however the prior art states a general simulation event, column 8, lines 20-25) in an electronic design automation (EDA) (COLUMN 2, LINE 51)) simulation environment (the specification defines the simulation as a broad category that is well known in the art, thus column 8, lines 20-25 teaches a general simulation event); simulating a second hardware component (specification fails to define what a first hardware component, but the prior art teaches examples of hardware component, column 3, lines 38-42) in the circuit design (known software circuit simulation, e.g., HDL, VHDL, column 5, lines 15-24) with a second

simulation model (the specification fails to define what a second simulation model is, however the prior art states a circuit verification method such as simulation, column 8, lines 12-22) in the EDA (COLUMN 2, LINE 51) environment; identifying state information (e.g., finite state machine, abstract, lines 22-25) comprising a transfer from the first simulation model (the specification fails to define what a first simulation model is, however the prior art states a general simulation event, column 8, lines 20-25)in the EDA (COLUMN 2, LINE 51) simulation environment (the specification defines the simulation as a broad category that is well known in the art, thus column 8, lines 20-25 teaches a general simulation event), said transfer being directed to the second simulation model (the specification fails to define what a second simulation model is, however the prior art states a circuit verification method such as simulation, column 8, lines 12-22) in a receiving the state information (e.g., finite state machine, abstract, lines 22-25) from the first simulation model; and making the state information (e.g., finite state machine, abstract, lines 22-25) available to the second simulation model (the specification fails to define what a second simulation model is, however the prior art states a circuit verification method such as simulation, column 8, lines 12-22)without simulating the transfer in the circuit design (known software circuit simulation, e.g., HDL, VHDL, column 5, lines 15-24).

Claim 2. The method of claim 1 wherein simulating the transfer from the first simulation model (the specification fails to define what a first simulation model is, however the prior art states a general simulation event, column 8, lines 20-25) to the second simulation

model (the specification fails to define what a second simulation model is, however the prior art states a circuit verification method such as simulation, column 8, lines 12-22) in the circuit design (known software circuit simulation, e.g., HDL, VHDL, column 5, lines 15-24) comprises transferring the state information (e.g., finite state machine, abstract, lines 22-25) through at least one additional simulation model in the EDA (COLUMN 2, LINE 51) simulation environment (the specification defines the simulation as a broad category that is well known in the art, thus column 8, lines 20-25 teaches a general simulation event).

Claim 3. The method of claim 1 wherein receiving the state information (e.g., finite state machine, abstract, lines 22-25) and making the state information (e.g., finite state machine, abstract, lines 22-25) available comprises: storing the state information (e.g., finite state machine, abstract, lines 22-25) in a coherent state memory space that is part of the EDA (COLUMN 2, LINE 51) simulation environment (the specification defines the simulation as a broad category that is well known in the art, thus column 8, lines 20-25 teaches a general simulation event) and corresponds to an element in the circuit design (known software circuit simulation, e.g., HDL, VHDL, column 5, lines 15-24) being simulated, said coherent state of memory space being accessible to both the first simulation model (the specification fails to define what a first simulation model is, however the prior art states a general simulation event, column 8, lines 20-25)and the second simulation model.

Claim 5. The method of claim I wherein receiving the state information (e.g.,

finite state machine, abstract, lines 22-25) and making the state information (e.g., finite state machine, abstract, lines 22-25) available comprises at least one of a virtual transfer path for use when a simulation model of a transfer path in the circuit design (known software circuit simulation, e.g., HDL, VHDL, column 5, lines 15-24) is not included in the EDA (COLUMN 2, LINE 51) simulation environment (the specification defines the simulation as a broad category that is well known in the art, thus column 8, lines 20-25 teaches a general simulation event); and a higher performance transfer path than the simulation model of the transfer path in the circuit design (known software circuit simulation, e.g., HDL, VHDL, column 5, lines 15-24).

Claim 7. The method of claim 3 wherein the EDA (COLUMN 2, LINE 51) simulation environment (the specification defines the simulation as a broad category that is well known in the art, thus column 8, lines 20-25 teaches a general simulation event) comprises a plurality of additional simulation models, each of the plurality of additional simulation models corresponding to one or more of a plurality of additional coherent state memory spaces, the method further comprising: identifying additional state information (e.g., finite state machine, abstract, lines 22-25) comprising additional transfers among the plurality of additional simulation models in the EDA (COLUMN 2, LINE 51) simulation environment (the specification defines the simulation as a broad category that is well known in the art, thus column 8, lines 20-25 teaches a general simulation event); and storing the additional state information (e.g., finite state machine, abstract, lines 22-25) in appropriate ones of the plurality of additional coherent state

memory spaces such that the additional state information (e.g., finite state machine, abstract, lines 22-25) is accessible to corresponding ones of the plurality of additional simulation models without simulating the additional transfers in the circuit design (known software circuit simulation, e.g., HDL, VHDL, column 5, lines 15-24).

Claim 12. The method of claim 11 wherein the logic simulator comprises one of a hardware description language (HDL) (known software circuit simulation, e.g., HDL, VHDL, column 5, lines 15-24) based simulator, a gate-level simulator, a simulation accelerator, a system simulator, a cycle simulator, and a programmable hardware emulator.

Claim 13. The method of claim 11 wherein the programming language simulator comprises at lease one of a C programming language simulator, (column 6, lines 27-2) a C++ programming language simulator, a simulator using a C-based language, a simulator using a C++ based language, and a JAVA programming language simulator.

Claim 14. The method of claim 9 wherein the hardware simulation domain comprises at least one simulation model of a circuit element in the circuit design (known software circuit simulation, e.g., HDL, VHDL, column 5, lines 15-24).

Claim 15. The method of claim 8 further comprising: partitioning the circuit design (known software circuit simulation, e.g., HDL, VHDL, column 5, lines 15-24) into the plurality of simulation domains based on a partition criteria.

Claim 16. The method of claim 15 wherein the partition criteria comprises at least

one of an abstraction (column 5, lines 46-51) level, a simulation type, and a function type.

Claim 17. The method of claim 16 wherein partitioning the circuit design (known software circuit simulation, e.g., HDL, VHDL, column 5, lines 15-24) based on the abstraction (column 5, lines 46-51) level partitions the circuit design (known software circuit simulation, e.g., HDL, VHDL, column 5, lines 15-24) into at least one of a pin-level domain, a bus-level domain, and a transaction-level domain.

Claim 18. The method of claim 16 wherein partitioning the circuit design (known software circuit simulation, e.g., HDL, VHDL, column 5, lines 15-24) based on the simulation type partitions the circuit design (known software circuit simulation, e.g., HDL, VHDL, column 5, lines 15-24) into at least one of a software execution domain, a logic simulator domain, and a programming language simulator domain.

Claim 19. The method of claim 16 wherein partitioning the circuit design (known software circuit simulation, e.g., HDL, VHDL, column 5, lines 15-24) based on the function type comprises: identifying one or more functional elements in the circuit design (known software circuit simulation, e.g., HDL, VHDL, column 5, lines 15-24) that have a particular level of independent operation from the remainder of the circuit design (known software circuit simulation, e.g., HDL, VHDL, column 5, lines 15-24); and defining a domain encompassing each identified functional element.

Claim 20. The method of claim 8 wherein each of the plurality of simulation domains provides a particular performance level and a particular resolution level, and wherein the particular simulation domains are selectively activated or deactivated during particular stages of simulation in combinations that either accelerate performance of the EDA (COLUMN 2, LINE 51) simulation environment (the specification defines the simulation as a broad category that is well known in the art, thus column 8, lines 20-25 teaches a general simulation event) or increase resolution of the EDA (COLUMN 2, LINE 51) simulation environment (the specification defines the simulation as a broad category that is well known in the art, thus column 8, lines 20-25 teaches a general simulation event).

Claim 21. The method of claim 8 wherein selectively activating and deactivating the particular simulation domains comprises: identifying a system state of the circuit design (known software circuit simulation, e.g., HDL, VHDL, column 5, lines 15-24); determining which of the plurality of simulation domains are to be active for the identified system state; and advancing simulation time only in each activated simulation domain.

Claim 24. The method of claim 22 wherein the system state comprises system addresses in the circuit design (known software circuit simulation, e.g., HDL, VHDL, column 5, lines 15-24).

Claim 30. The method of claim I wherein both the first simulation model (the

specification fails to define what a first simulation model is, however the prior art states a general simulation event, column 8, lines 20-25) and the second simulation model (the specification fails to define what a second simulation model is, however the prior art states a circuit verification method such as simulation, column 8, lines 12-22) are within a same simulation domain in the EDA (COLUMN 2, LINE 51) simulation environment (the specification defines the simulation as a broad category that is well known in the art, thus column 8, lines 20-25 teaches a general simulation event).

Claim 31. The method of claim I wherein the first simulation model (the specification fails to define what a first simulation model is, however the prior art states a general simulation event, column 8, lines 20-25) and the second simulation model (the specification fails to define what a second simulation model is, however the prior art states a circuit verification method such as simulation, column 8, lines 12-22) are within different simulation domains in the EDA (COLUMN 2, LINE 51) simulation environment (the specification defines the simulation as a broad category that is well known in the art, thus column 8, lines 20-25 teaches a general simulation event).

Claim 32. A method comprising: simulating a first abstraction (column 5, lines 46-51) level of a circuit functionality in a circuit design (known software circuit simulation, e.g., HDL, VHDL, column 5, lines 15-24) with a first simulation model (the specification fails to define what a first simulation model is, however the prior art states a general simulation event, column 8, lines 20-25) in an electronic design automation (EDA (COLUMN 2, LINE 51)) simulation environment (the specification defines the simulation

as a broad category that is well known in the art, thus column 8, lines 20-25 teaches a general simulation event): simulating a second abstraction (column 5, lines 46-51) level of the circuit functionality in the circuit design (known software circuit simulation, e.g., HDL, VHDL, column 5, lines 15-24) with a second simulation model (the specification fails to define what a second simulation model is, however the prior art states a circuit verification method such as simulation, column 8, lines 12-22)in the EDA (COLUMN 2, LINE 51) environment; reading state information (e.g., finite state machine, abstract, lines 22-25) from the first simulation model (the specification fails to define what a first simulation model is, however the prior art states a general simulation event, column 8, lines 20-25)in the EDA (COLUMN 2, LINE 51) simulation environment (the specification defines the simulation as a broad category that is well known in the art, thus column 8, lines 20-25 teaches a general simulation event) when a simulation domain of the first simulation model (the specification fails to define what a first simulation model is, however the prior art states a general simulation event, column 8, lines 20-25) is deactivated; and writing the state information (e.g., finite state machine, abstract, lines 22-25) to the second simulation model (the specification fails to define what a second simulation model is, however the prior art states a circuit verification method such as simulation, column 8, lines 12-22)in the EDA (COLUMN 2, LINE 51) simulation environment (the specification defines the simulation as a broad category that is well known in the art, thus column 8, lines 20-25 teaches a general simulation event) prior to activation of a simulation domain of the second simulation model.

Claim 33. The method of claim 32 wherein the first simulation model (the specification fails to define what a first simulation model is, however the prior art states a general simulation event, column 8, lines 20-25) and the second simulation model (the specification fails to define what a second simulation model is, however the prior art states a circuit verification method such as simulation, column 8, lines 12-22) each have a particular level of performance and resolution, and wherein simulation of the circuit design (known software circuit simulation, e.g., HDL, VHDL, column 5, lines 15-24) switches from the first simulation model (the specification fails to define what a first simulation model is, however the prior art states a general simulation event, column 8, lines 20-25)to the second simulation model (the specification fails to define what a second simulation model is, however the prior art states a circuit verification method such as simulation, column 8, lines 12-22)is based on a change in a performance level and/or a resolution level desired at a different stage of simulation.

Claim 35. A machine readable medium having stored thereon machine executable instructions that when executed implement a method comprising: simulating a first hardware component (specification fails to define what a first hardware component, but the prior art teaches examples of hardware component, column 3, lines 38-42) in a circuit design (known software circuit simulation, e.g., HDL, VHDL, column 5, lines 15-24) with a first simulation model (the specification fails to define what a first simulation model is, however the prior art states a general simulation event, column 8, lines 20-25)in an electronic design automation (EDA (COLUMN 2, LINE

51)) simulation environment (the specification defines the simulation as a broad category that is well known in the art, thus column 8, lines 20-25 teaches a general simulation event), simulating a second hardware component (specification fails to define what a first hardware component, but the prior art teaches examples of hardware component, column 3, lines 38-42)in the circuit design (known software circuit simulation, e.g., HDL, VHDL, column 5, lines 15-24) with a second simulation model (the specification fails to define what a second simulation model is, however the prior art states a circuit verification method such as simulation, column 8, lines 12-22)in the EDA (COLUMN 2, LINE 51) environment; identifying state information (e.g., finite state machine, abstract, lines 22-25) comprising a transfer from the first simulation model (the specification fails to define what a first simulation model is, however the prior art states a general simulation event, column 8, lines 20-25)in the EDA (COLUMN 2, LINE 51) simulation environment (the specification defines the simulation as a broad category that is well known in the art, thus column 8, lines 20-25 teaches a general simulation event), said transfer being directed to the second simulation model (the specification fails to define what a second simulation model is, however the prior art states a circuit verification method such as simulation, column 8, lines 12-22)in-a receiving the state information (e.g., finite state machine, abstract, lines 22-25) from the first simulation model; and making the state information (e.g., finite state machine, abstract, lines 22-25) available to the second simulation model (the specification fails to define what a second simulation model is, however the prior art states a

circuit verification method such as simulation, column 8, lines 12-22)without simulating the transfer in the circuit design (known software circuit simulation, e.g., HDL, VHDL, column 5, lines 15-24).

Claim 36. A machine readable medium having stored thereon machine executable instructions that when executed implement a method comprising: simulating a first abstraction (column 5, lines 46-51) level of a circuit functionality in a circuit design (known software circuit simulation, e.g., HDL, VHDL, column 5, lines 15-24) with a first simulation model (the specification fails to define what a first simulation model is, however the prior art states a general simulation event, column 8, lines 20-25) in an electronic design automation (EDA (COLUMN 2, LINE 51)) simulation environment (the specification defines the simulation as a broad category that is well known in the art, thus column 8, lines 20-25 teaches a general simulation event); simulating a second abstraction (column 5, lines 46-51) level of the circuit functionality in the circuit design (known software circuit simulation, e.g., HDL, VHDL, column 5, lines 15-24) with a second simulation model (the specification fails to define what a second simulation model is, however the prior art states a circuit verification method such as simulation, column 8, lines 12-22)in the EDA (COLUMN 2, LINE 51) environment; reading state information (e.g., finite state machine, abstract, lines 22-25) from the first simulation model (the specification fails to define what a first simulation model is, however the prior art states a general simulation event, column 8, lines 20-25)in the EDA (COLUMN 2, LINE 51)

simulation environment (the specification defines the simulation as a broad category that is well known in the art, thus column 8, lines 20-25 teaches a general simulation event) when a simulation domain of the first simulation model (the specification fails to define what a first simulation model is, however the prior art states a general simulation event, column 8, lines 20-25)is deactivated; and writing the state information (e.g., finite state machine, abstract, lines 22-25) to the second simulation model (the specification fails to define what a second simulation model is, however the prior art states a circuit verification method such as simulation, column 8, lines 12-22) in the EDA (COLUMN 2, LINE 51) simulation environment prior to activation of a simulation domain of the second simulation model.

Section III: Response to Arguments

103(a)

10. Applicants' arguments see pages 10-21, filed 05/08/2007, with respect to the rejections of claims 1-31 under 103(a) has been fully persuasive and considered. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground of rejection is made in view of Markov.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mr. Tom Stevens whose telephone number is 571-272-3715.

If attempts to reach the examiner by telephone are unsuccessful, please contact examiner's supervisor Mr. Anthony Knight 571-272-3687. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov.. Answers to questions regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) (toll-free (866-217-9197)).

Anthony Knight
Supervisory Patent Examiner
Tech Center 2100